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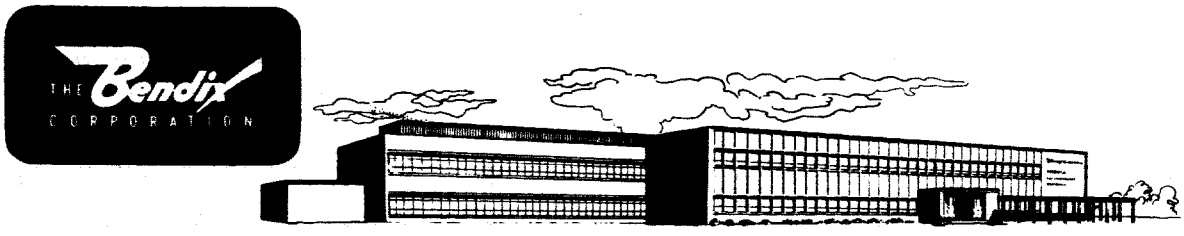
STUDY TO INVESTIGATE THE EFFECTS OF IONIZING RADIATION ON TRANSISTOR SURFACES

Contract NAS 8-20135

THIRD QUARTERLY REPORT FOR THE PERIOD ENDED MARCH 31, 1966



RESEARCH LABORATORIES DIVISION

SOUTHFIELD, MICHIGAN

Bendix Project 2400

Report No. 3434

STUDY TO INVESTIGATE THE EFFECTS OF IONIZING RADIATION ON TRANSISTOR SURFACES

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May 1966

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama 35812, Attn: PR – EC

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FOREWORD

The program whose status is described in this report is being performed for NASA, Marshall Space Flight Center, Astrionics Laboratory, for the purpose of delineating the effects of ionizing radiation on transistor surfaces. The work involves identifying and characterizing the mechanisms producing the effects, establishing models which describe the physical phenomena, developing nondestructive screening techniques which enable separating transistors with good immunity from radiation surface effects from those with poor immunity, and evaluating which, if any, surface treatments or manufacturing processes lead to a minimum of ionizing radiation surface effects.

The experimental portion of the program is conducted with 150 kv X-rays as the source of ionizing radiation. This radiation source is energetic enough to penetrate the transistor can and produce surface ionization, but not energetic enough to produce bulk transistor damage which would unduly complicate the results by combining surface and bulk damage. Extensive use is made of low current surface behavior which accentuates the phenomena, and various bias conditions which serve to enhance or suppress the different mechanisms.

Phase I of the program is devoted to studying a single transistor type under a variety of conditions for the purpose of identifying the mechanisms, establishing the models and understanding surface behavior under thermal, electrical or ionizing radiation stresses. Phase II involves the evaluation of a variety of transistors with different surface treatments, construction techniques and manufacturing processes. Results of this evaluation coupled with Phase I results will lead to recommendations for screening techniques and for device construction to minimize surface radiation effects.

SECTION 1

INTRODUCTION AND SUMMARY

This report presents the results obtained during the third quarterly period of investigation, a summary of the Phase I results and the plans for Phase II. Six tests were conducted on Fairchild 2N1613 transistors during this period to complement tests performed during the second quarter and to investigate several new areas. Tests included investigations of:

(1) Bias effects during irradiation using series testing

(2) Use of junction capacitance measurements for channel detection

(3) Temperature coefficients of damage

(4) Ionizing rate effects

(5) Reverse junction V-I characteristics

(6) Temperature recovery cycles

(7) Techniques for identification of damage mechanisms.

These investigations concluded the Phase I portion of the program, with the exception of irradiation testing of evacuated devices. This test has been delayed due to difficulties in fabrication of the hard vacuum envelopes.

Based on the results of Phase I, a general test procedure has been designed for the various semiconductor devices to be evaluated in Phase II, which will lead to: (a) determination of mechanisms of h_{FE} and I_{CBO} degradations, (b) determination of the relative magnitudes of various mechanisms at small and large doses, and (c) evaluation of the effectiveness of the temperature recovery cycle as a screening tool.

SECTION 2

THIRD-QUARTER TESTS

Six X-ray tests were conducted during this period to identify mechanisms and investigate bias effects, temperature recovery, and ionizing rate effects. Tests were performed to investigate new areas, such as temperature coefficient of damage, reverse junction V-I characteristics, and correlation of temperature and ionization induced damage, and to clarify observations made in earlier tests.

2.1 TEST 5

Phase I parallel mode test results showed damage-dose characteristics of transistors that were functions of their histories of bias-radiation stresses and recovery stresses. In a parallel mode test, a separate device is used for each stress under study. Because transistors may differ in their sensitivities to a particular stress, the results of parallel mode tests are, to a large extent, qualitative. Test 5, a series test consisting of several irradiation periods followed by temperature recovery periods, was devised to obtain a more quantitative picture of damage buildup as a function of various bias-radiation stresses. The damages of particular interest in this test were gain degradation and increased I_{CBO} resulting from combined ionizing radiation and electrical bias stresses.

The major objective of the test was to determine the different effects of various bias-radiation stresses on the same device. The investigation included periods of X-ray irradiation at three different rates to obtain data on radiation rate effects. Other objectives were to investigate temperature coefficient of damage and changes in emitter-base and collector-base junction capacitances as functions of bias and dose.

Two devices were selected for the series test: one transistor had an extensive history of radiation testing, and the second was a new device. During the first part of this three-part test, both devices were subjected to the same series of bias-radiation stresses at the maximum available radiation rate ($\dot{\phi}_{max} \doteq 5 \times 10^5$ r/hr) alternated with high

temperature recovery periods (300°C for 5 hrs). The test sequence is indicated below by showing the bias condition used during each period of the test followed by an R to indicate a recovery period.

(a) Passive - R, (b) V_{CB} = +12 V - R, (c) V_{CB} = +6 V - R,
(d) V_{CB} = +50 V - R, (e) Active, V_{CB} = +6 V, I_E = 10 mA - R,
(f) Saturation, I_C = 10 mA, I_B = 2 mA - R, (g) V_{EB} = +3 V - R.

For the second part of the test, the radiation rate was reduced to $\dot{\phi} = 0.1\ \dot{\phi}_{max}$. Both devices were irradiated until the rate of damage buildup became quite small; the first device was biased V_{CB} = +50 V, and the second device was passive during irradiation. Both transistors were then recovered.

The radiation rate was reduced to $\dot{\phi} = 0.01\ \dot{\phi}_{max}$ for the third part of the test. The bias conditions were the same as those used in part 2 of the test, and the bias radiation stresses were continued until the rate of damage buildup was very small compared with initial damage buildup rate.

The effects of various bias conditions on damage buildup during radiation may be readily observed by referring to Figures 1 and 2, which show the relative buildup of gain degradation, and Figures 3 and 4, which show relative buildup of I_{CBO}. Reverse biases on the emitter-base junctions cause fast initial damage buildup, while forward biases on junctions tend to ameliorate damage buildup rate. This may be seen in Figures 1 and 2 by observing that the active damage response builds up more slowly and remains less extensive than the response for V_{CB} = +6 V although the collector-base bias was the same in both cases.

The high peaking responses of the I_{CBO} curves of Figure 4 indicate the presence of a large number of generation sites when a channel is present in Device 8. These curves may be contrasted with those of Figure 3 for identical stress conditions. Although the relative magnitudes of the damage response curves for both transistors correspond generally according to the bias used, no large generation sites were apparent in Device 15 when the channel was present.

Although transistors exhibit different sensitivities to bias-radiation stresses, thereby causing damage response curves to occur in somewhat different rank order of magnitude from device to device, in general the I_{CBO} response curves occur in very nearly the same order as the gain

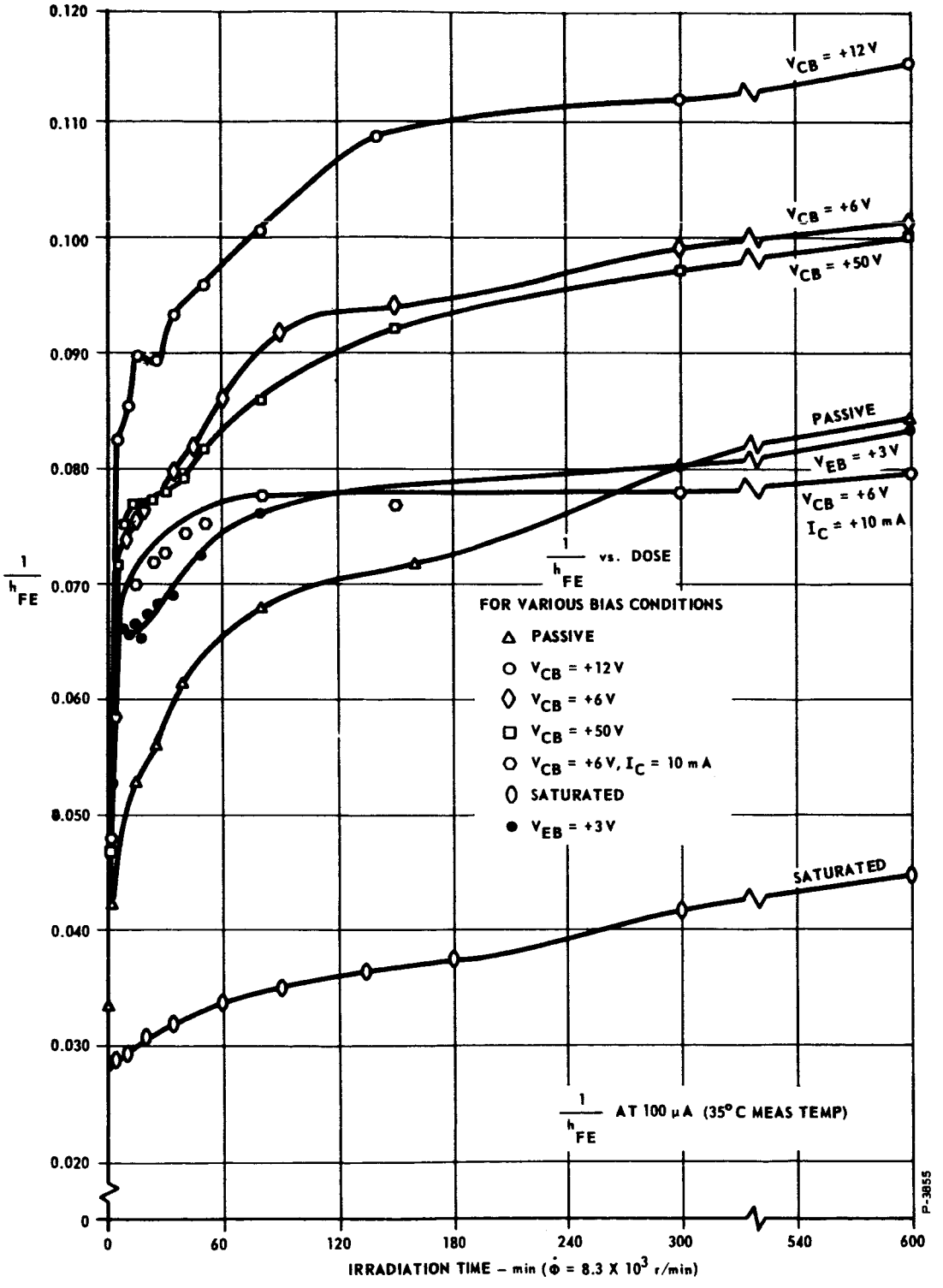


Figure 1 - Effects of Bias During Irradiation on Low Current h_{FE} Damage Buildup - Device 15

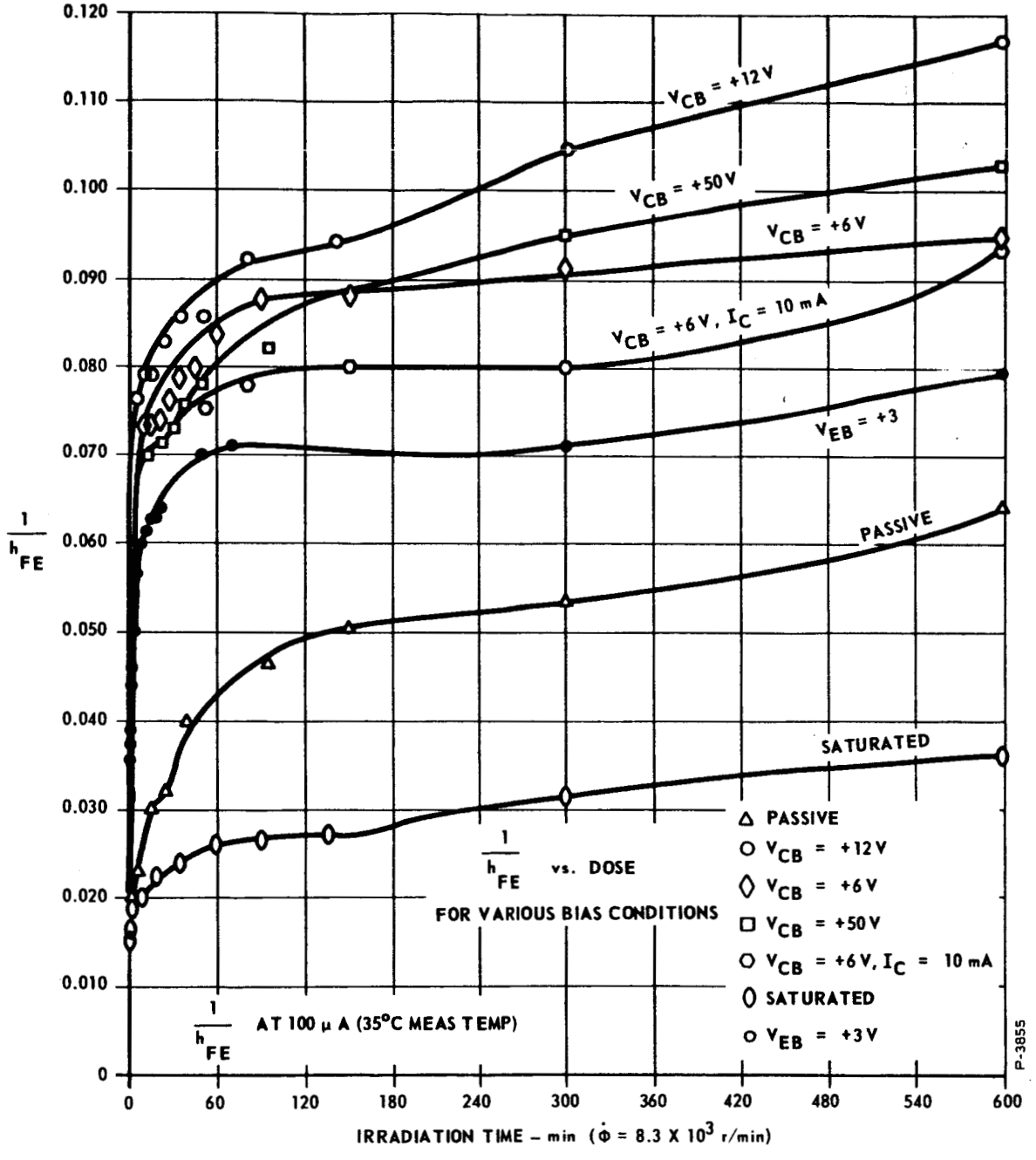


Figure 2 - Effects of Bias During Irradiation on Low Current h_{FE} Damage Buildup - Device 8

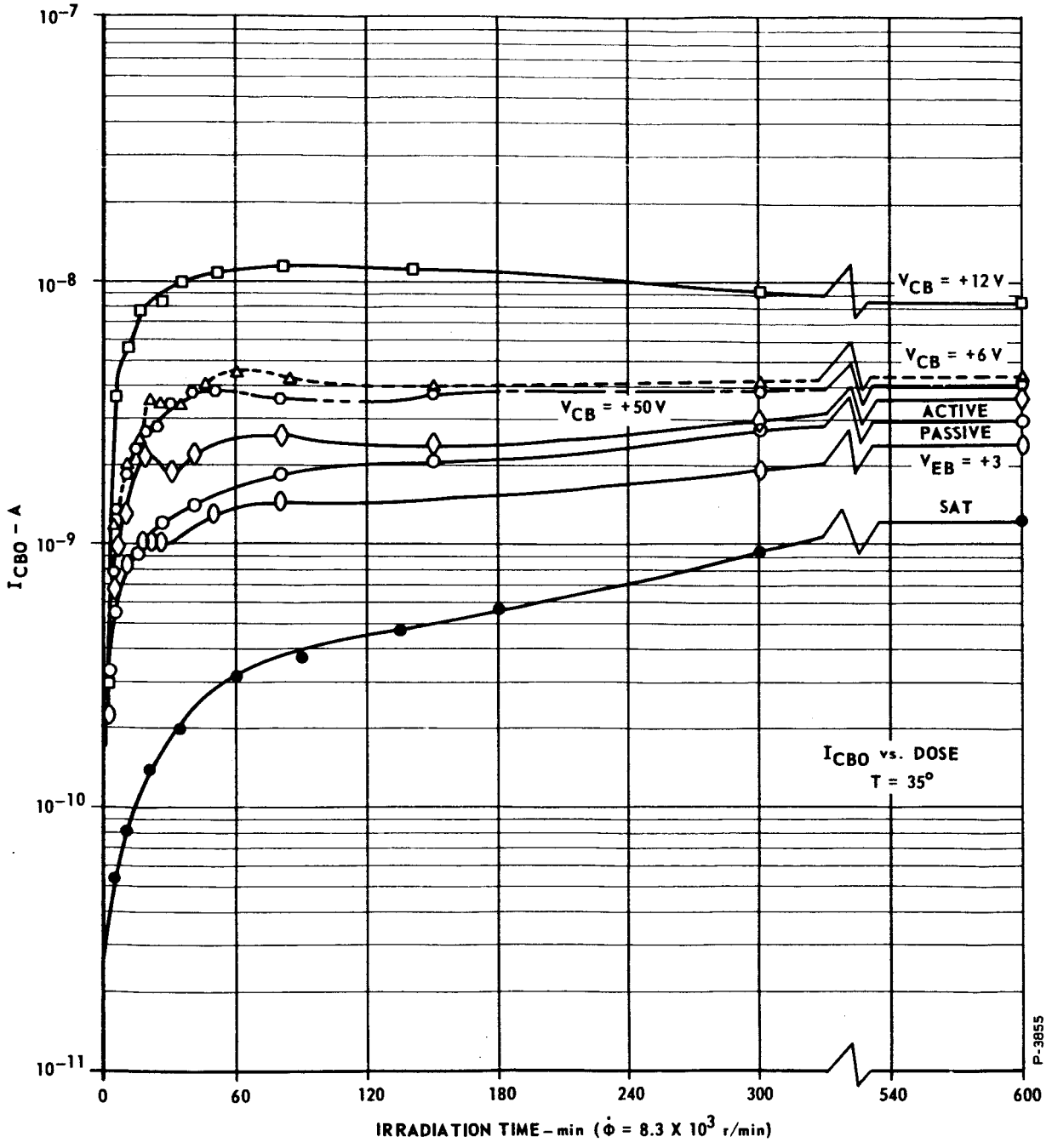


Figure 3 - Effects of Bias During Irradiation on I_{CBO} Buildup - Device 15

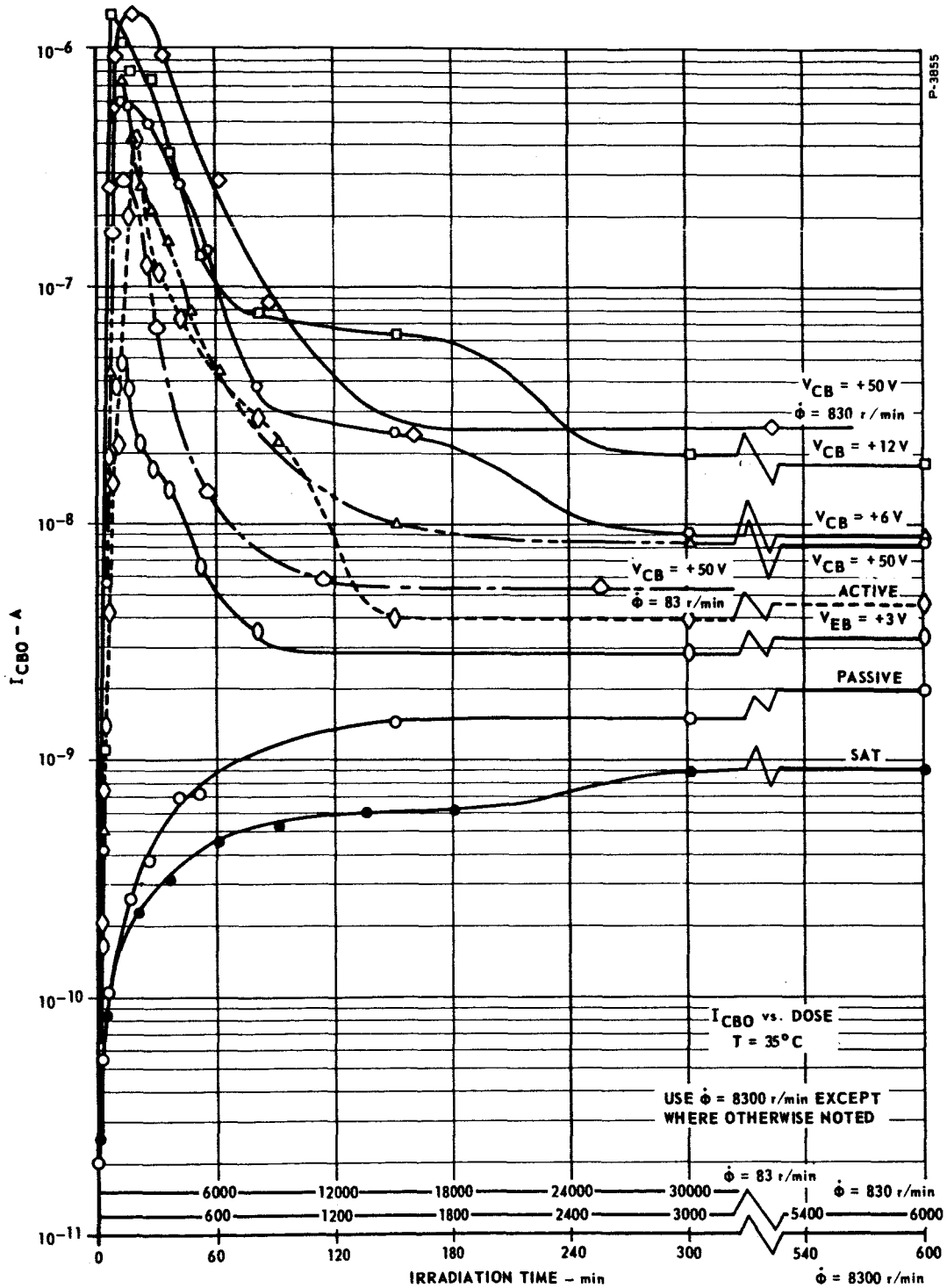


Figure 4 - Effects of Bias During Irradiation on I_{CBO} Buildup - Device 8

damage response curves and sustain more damage when the collector-base junction is reverse-biased during irradiation. The apparent anomaly that the greatest collector-base reverse bias (V_{CB} = +50 V) during irradiation does not cause the greatest damage suggests that increased reverse bias beyond some limiting point causes opposing mechanisms to occur which tend to diminish total damage. Perhaps when a great enough reverse bias is applied so that inversion of the base region beneath the surface begins before appreciable charge migration occurs in the oxide, a competitive process results that reduces damage. Section 3.3 presents a discussion of the model for this phenomenon.

Junction capacitance measurements have provided an excellent means of monitoring the formation and decay of a channel. The magnitude of the capacitance measurement, however, is not indicative of the magnitude the leakage, as is evident from Figure 5, which shows that the device which had the larger collector-base capacitance while the channel existed, had the smaller leakage current. This enforces the theory that channel plus generation sites[1] are required for large leakage currents.

Damage buildup in transistors appears to be radiation rate sensitive. Figure 6 shows the buildup of gain damage at 100 μA measurement current for the three rates used in the test. The results show that for a test transistor biased with V_{CB} = +50 V, the two lower rates produced damage that exceeded the maximum rate damage at equivalent doses. Figures 4 and 7 show the dose rate effects on I_{CBO} for the same device at early doses, and Figure 8 shows the corresponding collector-base capacitances as functions of the dose rate. These figures indicate that the collector-base capacitance and I_{CBO} curves for $\phi = \phi_{max}$ fall between the curves for $\phi = 0.1\ \phi_{max}$ and for $\phi = 0.01\ \phi_{max}$, even though the gain damage response curves for both reduced rates are almost the same.

Figure 9 indicates the radiation rate sensitivity of a transistor that is passive during irradiation by showing the effects of rate on I_{CBO} buildup. It is noteworthy that a decrease of one decade in dose rate (from 5×10^4 r/hr to 5×10^3 r/hr) produces a larger reverse leakage. This type of behavior is also observable for the reverse biased transistor in Figures 7, 8 and 9.

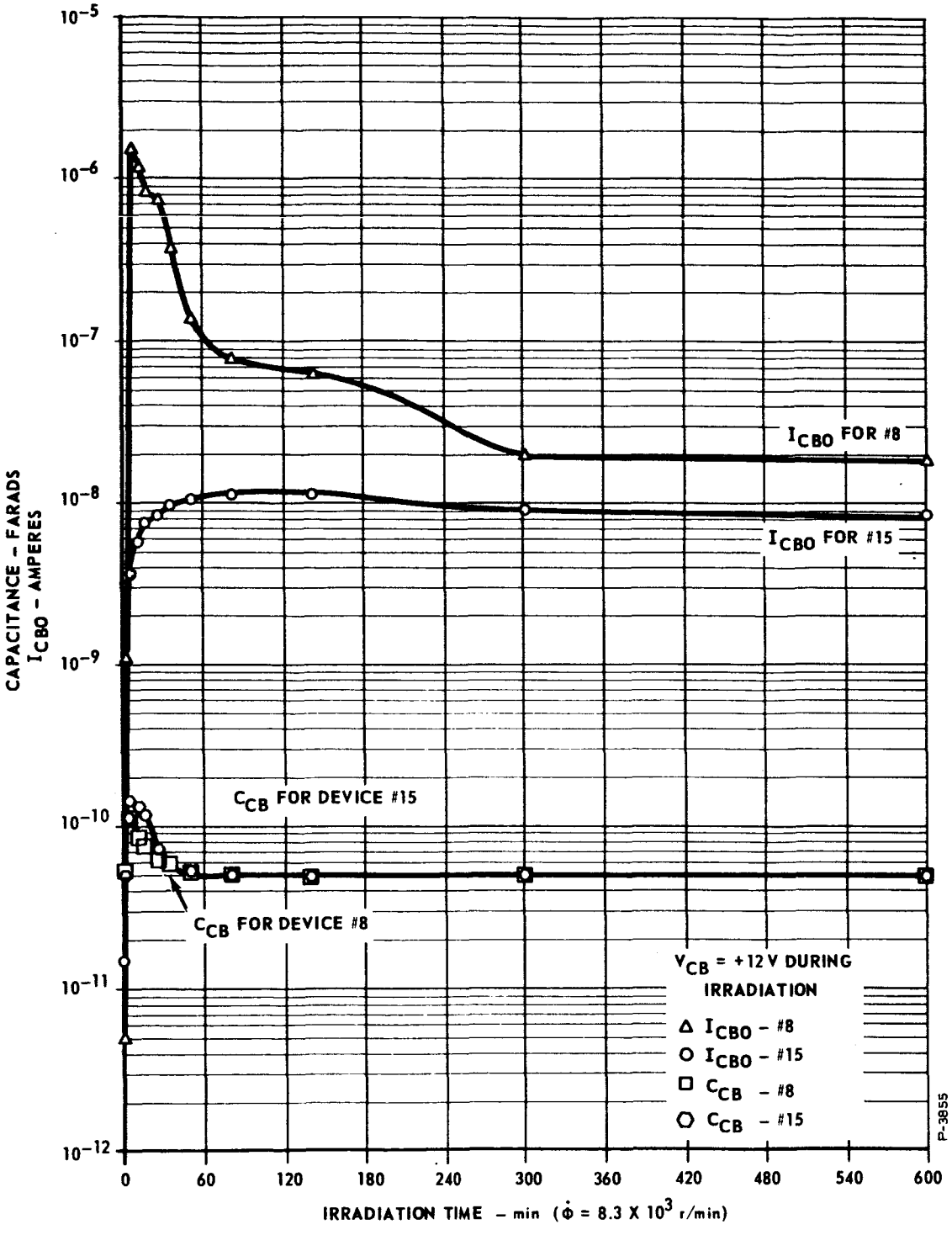


Figure 5 - I_{CBO} and C_{CB} Versus Dose - Devices 8 and 15

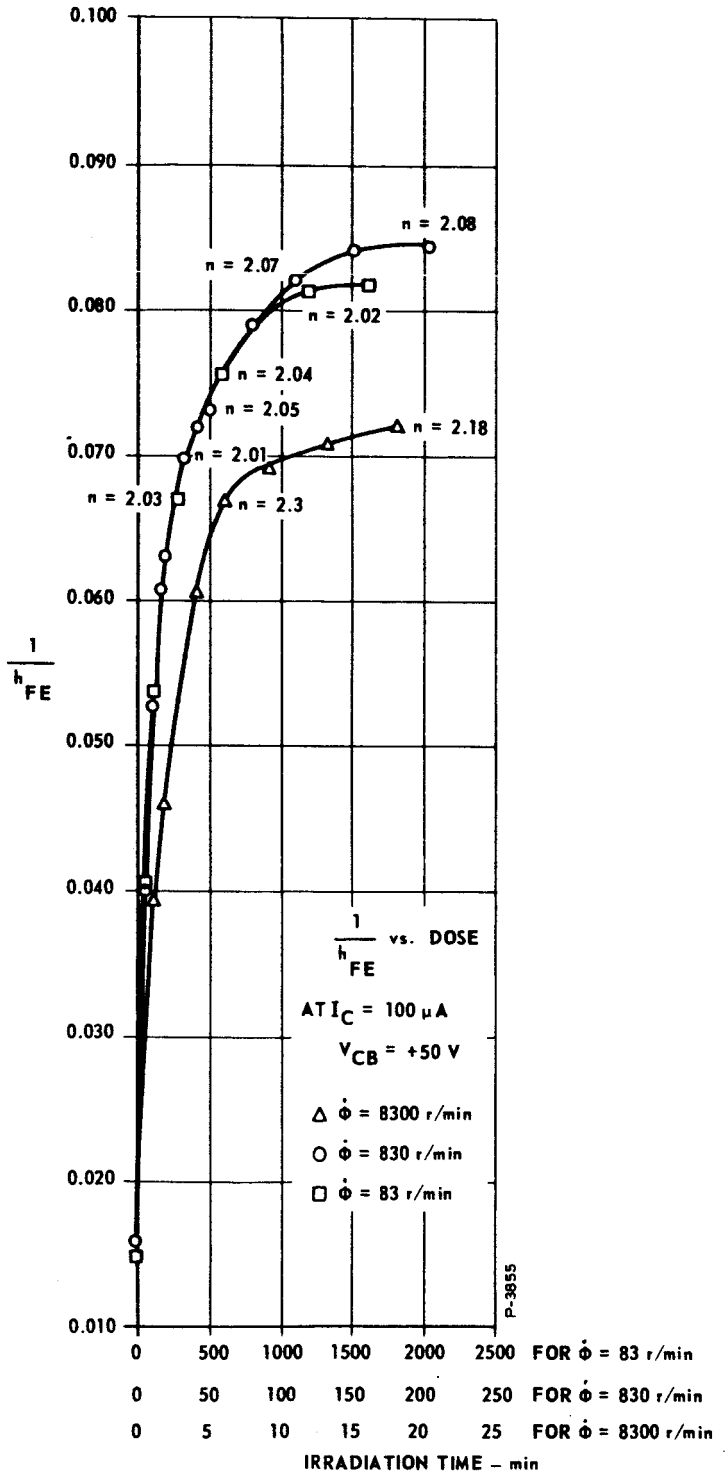


Figure 6 - Dose Rate Effects on Gain Damage - Device 8

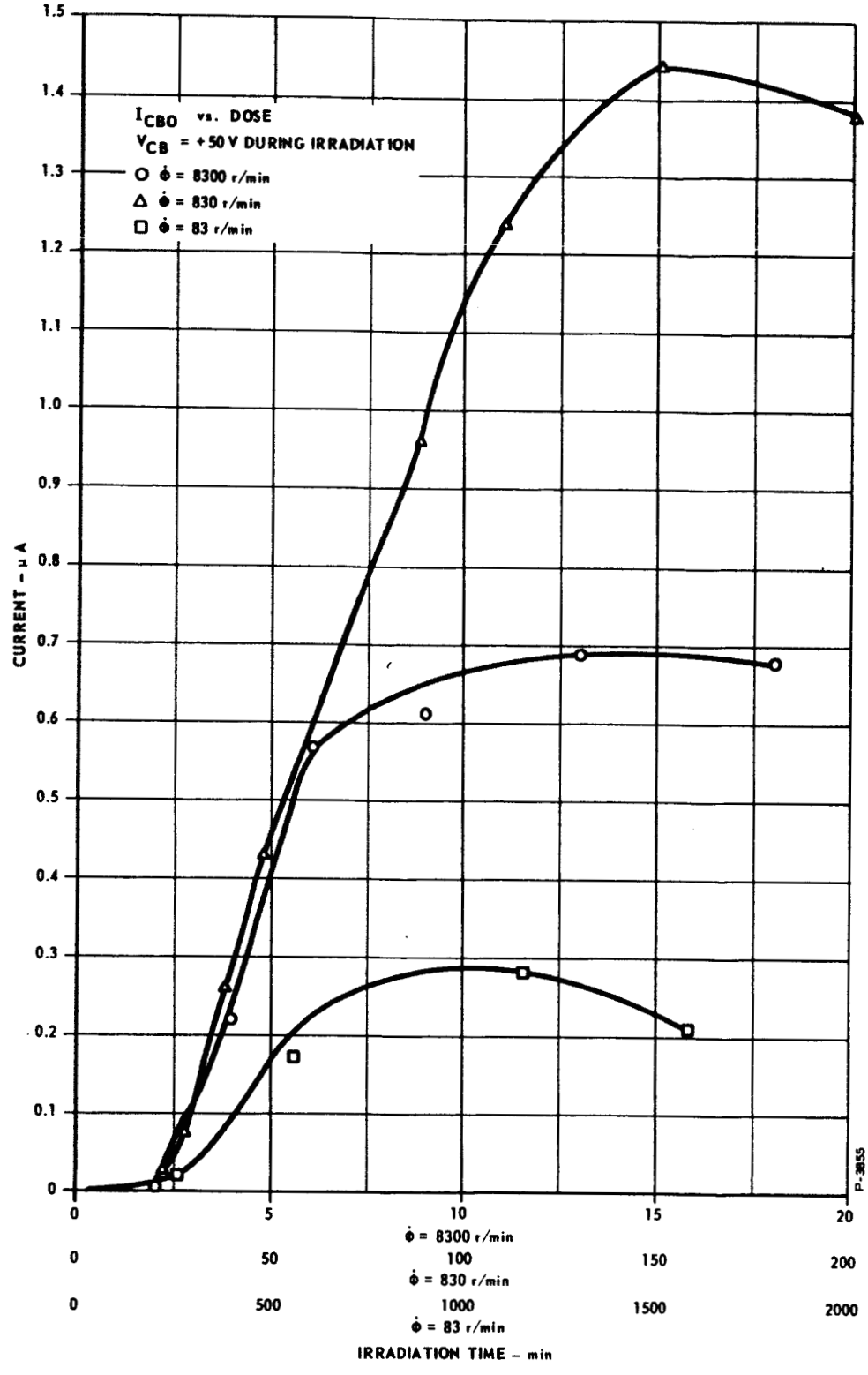


Figure 7 - Dose Rate Effects on I_{CBO} - Device 8

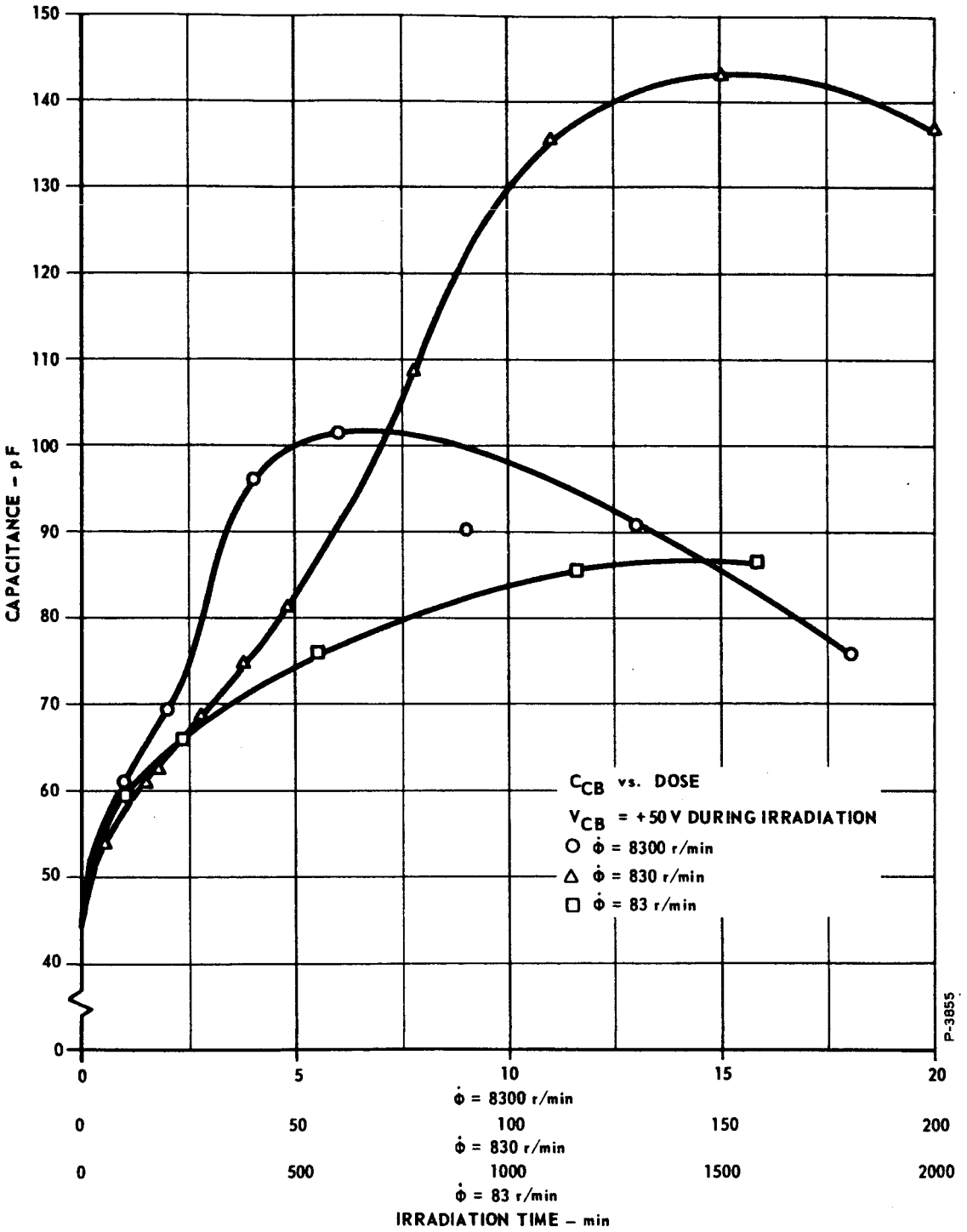


Figure 8 - C_{CB} as a Function of Dose Rate - Device 8

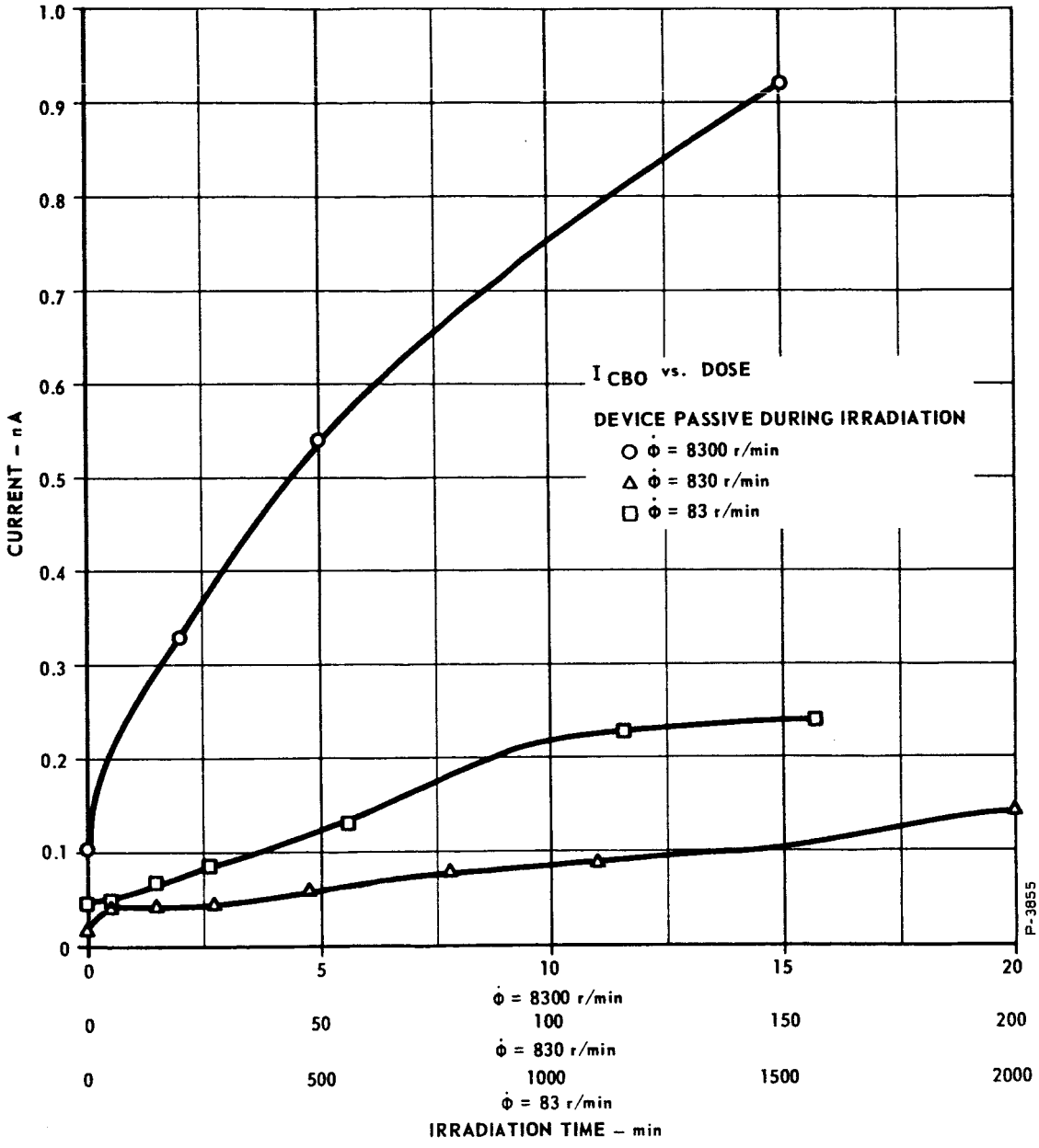


Figure 9 - I_{CBO} as a Function of Dose Rate - Device 15

The slope constant n*, useful for indicating the type of damage mechanism producing the damage, was computed at various data points for all three rates used in the test (refer to Figure 6). At $\dot{\phi} = 5 \times 10^5$ r/hr, n increased to approximately 2.3 when the channel was present (as verified by increased collector-base capacitance) and then returned to a value of 2.06 after the channel had receded. It is noteworthy that for both $\dot{\phi} = 5 \times 10^4$ and 5×10^3 r/hr, n values were never greater than 2.09 (significantly less than that for equivalent dose at $\dot{\phi} = 5 \times 10^5$ r/hr) even when the channel was present. This implies that n values significantly greater than 2 are a good indicator of the existence of a channel but that the converse is not true; i.e., a channel may exist even though the slope constant n is only very nearly 2, which was previously believed to indicate that no channel was present.

Data were recorded at 0°C and at 35°C before irradiation, when a channel was present at early dose (about 15 minutes at $\dot{\phi} = 5 \times 10^5$ r/hr) and at the end of each test period (600 minutes at $\dot{\phi} = 5 \times 10^5$ r/hr) for all bias-radiation stresses used in the test. Indications are that gain damage has a very large temperature coefficient (TC) when a channel is present and a very small TC at large doses. Much of the data is inconclusive because measuring h_{FE} produces an electrical stress which results in annealing damage out of the transistor, making it difficult to separate changes due to temperature variations from changes due to annealing. Test 10, which is discussed in Section 2.6, is a continuation of the investigation of TC.

2.2 TEST 6

The purpose of Test 6 was to investigate the possible correlation between temperature and X-ray induced damage. Attempts were made to induce surface degradation in test transistors by using a combination of reverse-biased junction and high temperature stresses, an established technique for evaluating device surfaces.

A single 2N1613 transistor was used as a pilot device to determine what effects could be expected from bias-temperature stresses. Bias, temperature and time conditions on the pilot device were: (a) $V_{EB} = 2$ V, T = 200°C, t = 30 minutes, (b) $V_{EB} = 5$ V, T = 200°C, t = 30 minutes, (c) $V_{EB} = 5$ V, T = 250°C, t = 33 minutes. Gain and leakage changes from original values were negligible for all conditions.

*The slope constant n is discussed in detail in the Second Quarterly Report beginning on page 3.

After a recovery period of baking passively at 300°C for 5 hours, the collector-base junction of the pilot was reverse-biased with 44 V and stressed for 37 minutes at 200°C, 5 minutes at 250°C, 5 minutes at 275°C, and 32 minutes at 300°C. Leakage current increased from 0.1 nA to 2.1 nA. The percent increases in gain degradation at 100 nA, 100 μA and 10 mA were 3.35 percent, 1.04 percent and 0.173 percent respectively.

The emitter-base junction was then reverse-biased at 5 V and stressed for 5 minutes at 250°C and 35 minutes at 290°C. h_{FE} at low measuring currents increased slightly, while h_{FE} at high measuring currents decreased slightly.

In an attempt to induce large changes such as those seen when X-rays are used to induce damage, the emitter-base junction was reverse-biased to breakdown (11.5 V) at 150 μA leakage current and baked at 250°C for 30 minutes. Increase in leakage current was negligible, but h_{FE} at 100 nA, 100 μA, and 10 mA decreased 47.7 percent, 12.0 percent, and 2.47 percent respectively. A significant point, which is emphasized, is that the gain degradation induced in the pilot transistor by bias-temperature stresses was permanent and therefore unlike X-ray damage.

As discussed above, very small damage changes occurred with reverse-biased junctions and high temperature stresses unless the junctions were biased to breakdown. Nevertheless, since changes did occur, attempts were made to correlate damage induced by temperature and X-ray. Ten transistors were reverse-biased with 5 V across the emitter-base and 50 V across the collector-base junctions and stressed at 290°C for 35 hours. The devices were then recovered, and bias-radiation stresses were applied with collector-base junctions reverse-biased at 12 V. An attempt was made to correlate device susceptibility to the two stresses by ranking the devices according to magnitude of h_{FE} and I_{CBO} changes due to temperature and radiation stresses, but no such correlation was found. Under X-ray stresses, all devices sustained degraded gain; while under temperature stresses, some devices exhibited gain degradation and others gain improvement.

2.3 TEST 7

Test 7 was a series test to determine what length of high temperature (320°C) recovery period is adequate to recover 2N1613 transistors that have incurred surface damage. Two devices were tested: one with

12 V reverse-biased collector-base junction and the other passive during irradiation. The transistors were irradiated for periods of 300 minutes (during which time data were recorded at 5 fixed points) alternated with various lengths of temperature recovery periods. The sequence of recovery periods used was 15 hours, 5 hours, 1/2 hour, 63 hours, 5 minutes, and 1 minute.

The data show that the length of the temperature recovery period required is somewhat dependent on the bias condition on the transistor during radiation. It was also noted that reirradiation of the device reverse-biased and temperature-recovered for less than 5 hours, produced minor variations in damage versus dose curves. No obvious advantage was found in the very long bakes; however, the extremely short bakes were undesirable since complete recovery was not achieved. In the passively irradiated device, I_{CBO} and h_{FE} characteristics recovered at about 1/2 hour, but baking for an additional 4 1/2 hours was not deleterious to recovery. As a result, a 5-hour recovery period at a temperature of about 300°C appears to be a satisfactory recovery period.

2.4 TEST 8

The purpose of this test was to investigate the changes in reverse-biased junction V-I characteristics due to ionizing radiation. Pre-irradiation reverse junction V-I characteristics were recorded for five test transistors using an X-Y plotter. Devices having bias conditions of passive, active (V_{CB} = +6 V, I_C = 3 mA), and V_{CB} = +12 V were irradiated long enough to induce a channel in those transistors with reverse-biased collector-base junctions. Reverse junction V-I characteristics were again recorded for all devices. The transistors were then subjected to bias-radiation stresses until the rate of change of damage (both gain and leakage) was very small. Final reverse junction V-I characteristics were plotted.

The reverse junction V-I characteristics are similar in shape regardless of the type of bias used during irradiation. Figures 10 and 11 are typical V-I characteristics for both junctions having had 12 V reverse collector bias. Both junction characteristics show increasing leakage current with dose, and the emitter-base breakdown voltage remains unchanged. Some collector-base junctions exhibited a large increase in I_{CBO} during a channel and then decreased when the channel receded, apparently due to the existence of a considerable number of

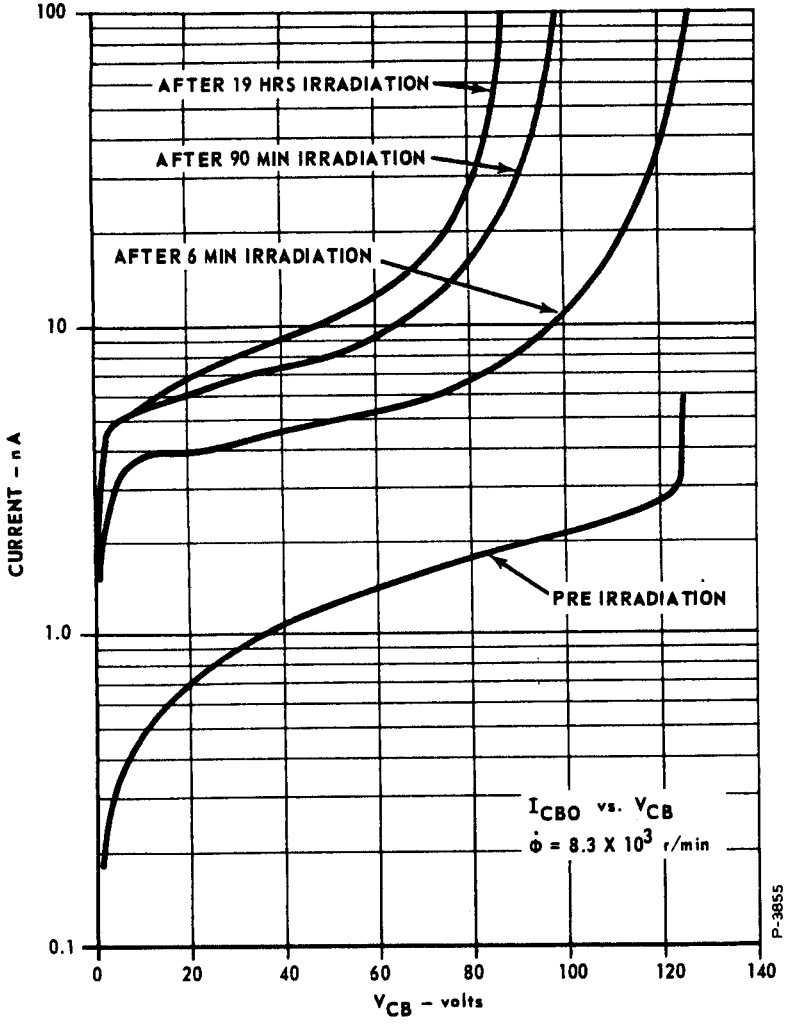


Figure 10 - Change in I_{CBO} as a Function of Dose - Device 15

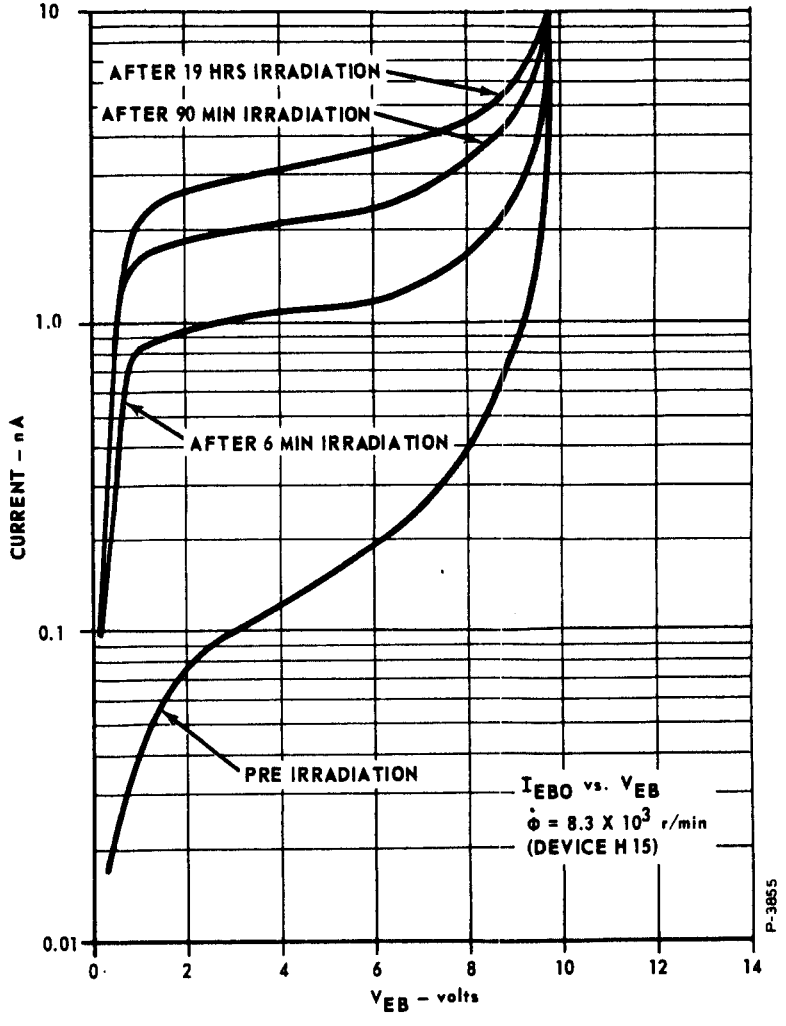


Figure 11 - Change in I_{EBO} as a Function of Dose - Device 15

generation sites. Although the breakdown of the collector-base junction exhibits softening, the breakdown remains the same as the original breakdown while the channel exists. It is noteworthy that the breakdown voltage decreases after the channel has receded, and the characteristic exhibits considerable softening of breakdown, indicating a significant decrease in surface breakdown voltage.

2.5 TEST 9

Gain damage, represented by $\Delta\frac{1}{h_{FE}}$, when plotted on a log scale as a function of the log I_C results in a linear curve over the range of $I_C = 10^{-3}$ A to $I_C = 10^{-7}$ A. Data from previous tests, e.g., Tests 1 and 5, revealed that such a plot departed from linearity at low measuring currents under some circumstances. This effect was described in Section 2.1 of the Second Quarterly Report and was called the "droop" effect. The objective of Test 9 was to investigate the "droop" characteristic.

Two transistors with their collector-base junctions reverse-biased were irradiated until channels were induced in each. The usual $\frac{1}{h_{FE}}$ data were recorded, and measurements were taken of V_{EB} and I_B for collector currents over the range of 3×10^{-4} to 10^{-10} A. When plotted on log-linear paper, no portion of the V_{EB}-I_B characteristic was obviously linear; i.e., I_B is not proportional to $\exp\frac{q\,V_{EB}}{n\,kT}$. The characteristic, log I_B as a function of V_{EB}, was a monotonically increasing curve having no straight line portion over the range from 10^{-9} to 3×10^{-5} A. The log-log plot of $\Delta\frac{1}{h_{FE}}$ as a function of I_C is a monotonically decreasing curve having no straight line portion over the range from 10^{-10} to 10^{-3} A. The effect of this behavior is to reduce the magnitude of n at low measurement currents.

2.6 TEST 10

The object of this test was to verify the existence of a temperature coefficient of damage. Data from Test 5 suggested the likelihood of a temperature coefficient, but the data were inconclusive because separation of changes of gain due to annealing of damage and to variations of temperature is difficult when damage is unstable. Test data showed that gain damage induced in transistors having only reverse-biased junctions during irradiation, is partially removed by the annealing

effects of the measuring currents. Transistors irradiated in an active mode, however, sustain gain degradation that is more stable, i.e., not as easily annealed by measurement.

The test transistor had an active bias of V_{CB} = +6 V, I_C = 10 mA during irradiation. Data were recorded at 0°C and 35°C before irridation, when a large channel was present, and when rate of damage change was very small.

The data clearly indicate that the damage has a very large temperature coefficient (>2%/°C) particularly at low measuring currents, when the channel is present. An extremely small temperature coefficient of damage (<0.2%/°C) was measured at large doses, after the channel had receded.

SECTION 3

PHASE I - SUMMARY

Phase I of the program has been completed except for one vacuum-irradiation test. Irradiation tests were performed on Fairchild 2N1613 silicon planar n-p-n transistors using 150 kv X-rays as the ionizing radiation source. Phase I studies and experiments have led to a detailed understanding of general surface behavior of transistors, and several mechanisms have been established which are instrumental in producing ionizing radiation surface effects which can affect the performance of a transistor over its entire electrical operating range. Device parameters investigated in this phase include: h_{FE}, I_{CBO}, BV_{CBO}, BV_{EBO}, C_{CB}, C_{EB} and V_{BE}.

A number of tests were performed to identify effects and mechanisms. The following paragraphs describe the major areas pursued.

3.1 AREAS OF INVESTIGATION

3.1.1 Electrical Bias Effects

The effects of several different electrical bias conditions during irradiation on h_{FE} and I_{CBO} degradation were investigated. Included were individual forward and reverse biases on the collector-base and base-emitter junctions, passive (no-bias), active (V_{CB} = 6 V, I_E = 10 mA), saturated and inverted (V_{EB} = 3 V, I_C = - 10 mA).

3.1.2 Time-Dose Relationships

The rate of damage buildup as a function of dose for several identifiable surface mechanisms was determined by measuring h_{FE} and I_{CBO} at intervals throughout irradiation periods. In addition, relationships between time and dose were investigated by irradiating at different ionizing rates. These relationships are useful in identifying surface mechanisms and determining the validity of extrapolating high dose-rate test results to lower dose-rate environments which may also be encountered in use.

3.1.3 Recovery Effects

The effects of temperature, electrical bias conditions, and a combination of X-rays and electrical bias conditions on the removal of ionizing radiation induced surface damage were investigated. The effectiveness of these techniques was compared to determine the method most suitable as a recovery cycle following an ionizing radiation screening test. The use of recovery to enable series testing of devices was also investigated.

3.1.4 Temperature-Ionization Relationships

A combination of high temperature and reverse junction bias has been established as an acceptable means of determining non-radiation surface stability of semiconductor devices. A test was performed to determine if a correlation exists between these surface instabilities and those encountered during X-ray irradiation.

3.1.5 Irradiation of Evacuated Devices

A portion of the damage due to irradiation is attributed to ionization of the gas ambient surrounding the silicon die in which the transistor is fabricated. A test has been designed which uses several devices in a hard vacuum to study damage buildup during irradiation. This test has not yet been performed due to difficulties in fabricating the glass vacuum envelopes; however, it will be performed as soon as satisfactory envelopes are completed.

3.2 RESULTS OF TESTS

3.2.1 General

Some conclusions about the general behavior of ionizing radiation surface effects were discussed in Section 3 of the Second Quarterly Report. A majority of the tests performed during the third quarter were intended to complement test results of the second quarter. A summary follows of the general behavior of surface effects as determined by the entire Phase I program.

3.2.2 Silicon Damage Mechanisms

Three different degradation mechanisms affecting h_{FE} and leakage currents have been identified. They are I_{srg} - surface

space charge recombination-generation current, I_{ch} - surface channel current and a high current mechanism. I_{srg} and I_{ch} both degrade gain at low measurement currents and increase I_{CBO} and I_{EBO}. The high current component affects gain only at high measurement currents and produces degradation similar to the common base spreading resistance effect.

I_{srg} and I_{ch} are similar, in that they both produce base current components varying exponentially with V_{BE}. They can be differentiated by their exponential slope constants since $1.5 < n_{srg} \lesssim 2$ and $2 < n_{ch}$. Since I_{ch} occurs during a channel or inversion of the base region, junction capacitance measurements which are useful for detecting channels can also be used to distinguish this component. A deviation from the exponential behavior described above is sometimes encountered for I_{ch}, producing a gradual decrease in n_{ch} at very low measuring current. This "droop" effect has not yet been explained.

As shown in Figures 10 and 11, I_{srg} and I_{ch} produce similar reverse junction V-I characteristics, the main difference being in their magnitudes. Both components also affect the collector-base junction breakdown voltage by producing a "soft" breakdown; however, the base-emitter breakdown is relatively unaffected.

3.2.3 Bias Effects

All three damage components discussed above are sensitive to electrical bias conditions during irradiation, but I_{srg} and I_{ch} are most affected in magnitude. A reverse bias on either junction is more damaging than no bias (passive) or a forward bias, with the least amount of damage produced when both junctions are forward biased (saturated). Passive and forward biased devices generally develop an I_{srg} component only, which builds up gradually with dose approaching a limiting level. This gradual increase in damage is accompanied by a gradual increase in n_{srg} from 1.5 to 2.0.

When a reverse junction bias is applied during irradiation, junction capacitances increase rapidly, indicating growth of a channel. This rapid growth of a channel is accompanied by a rapid increase in I_{CBO} and h_{FE} degradation, which can be identified as I_{ch} by an exponential slope constant n in excess of 2. After doses of the order of 10^5 r, the junction capacitances reach a peak and begin to decrease and approach their original values, indicating a recession of the channel. Accompanying this reduction in the channel is a decrease

of n and a large reduction in the rate of damage buildup. Some devices actually show a decrease in I_{CBO} and gain damage as the channel recedes. After large doses ($> 10^6$ r) the channel apparently disappears, leaving a damage component with a slope constant n of about 2 which indicates the presence of an I_{srg} component. Although these effects are produced by a reverse bias on either junction, the reverse bias on the collector base seems to be more effective in producing gain damage even though gain degradation is a base-emitter property.

The magnitude of collector-base reverse bias appears to be directly proportional to the magnitude of gain damage at low voltages; however, a high reverse bias voltage ($\sim$ 50 volts) can cause deviations from this behavior by producing less damage than that produced by 6 volts. An attempt to partially explain the effect of high reverse bias is given in Section 3.3, even though the effect is not well understood.

X-ray induced gain damage can be partially removed by the stress of the gain measurement cycle. The amount of damage reduction, varying from 1 percent to 20 percent for a single cycle, is strongly dependent on the electrical bias conditions during irradiation, being least stable when a reverse bias alone is present, and most stable when the device is irradiated with a forward biased junction. The instability apparently cannot be attributed to the presence or absence of a channel, I_{srg} or I_{ch} alone, since all of these mechanisms can be produced with or without a forward biased junction during irradiation. The temperature coefficient of gain for an unirradiated transistor is typically 0.5 to 0.7%/°C. An irradiated active device (V_{CB} = 6 V, I_E = 10 mA) which encounters both I_{ch} and I_{srg} damage components, has a large TC of gain damage ($> 2\%/°C$) when I_{ch} is the dominant gain damage component. When I_{srg} is dominant (after a large exposure), TC decreases to a very small value ($< 0.2\%/°C$).

3.2.4 Damage Recovery Effects

Two techniques for removal of ionizing radiation surface damage have been investigated, a temperature bake and a combination of large junction forward biases and X-ray irradiation. Both methods cause an apparent removal of gain degradation and I_{CBO} components; however, reirradiation of the devices produces a damage buildup characteristic significantly different from that produced first by the bias X-ray recovery cycle. Apparently this cycle alters the surface effects causing damage but does not return them to their preirradiation conditions.

A temperature bake in excess of 300°C for five hours produces more complete recovery than the X-ray bias technique. Although some variations are observed in the damage buildup by reir-radiation, they are small in comparison to those for the X-ray-electrical bias technique.

3.2.5 Variations in Device Sensitivity

Large variations of sensitivity to ionizing radiation have been observed in devices of the same type. The variation of I_{CBO} produced during a channel is shown in Figures 3 and 4 for two similar devices. Junction capacitance measurements indicate that the channels are of approximately the same size; however, the two I_{CBO}'s are orders of magnitude apart. The more sensitive of these devices exhibits a large peak in I_{CBO} when C_{CB} peaks, tracking closely the shape of the C_{CB} curve. This behavior is best explained by the presence of "generation sites"[1] at the SiO_2-Si interface, which are not effective until a channel extends the collector-base junction to sites. It is interesting to note that gain damage indicates no such generation sites near the base-emitter junction for these two devices.

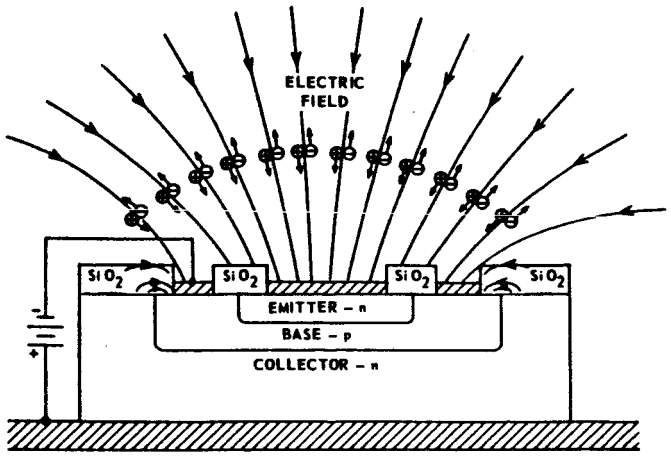
3.2.6 Rate Effects

Variations of damage versus dose curves for three ionizing rates: 5×10^5 r/hr, 5×10^4 r/hr and 5×10^3 r/hr, were studied. Test results indicate that damage is dependent on rate; however, no consistent conclusions can be drawn about the effect of rate on damage mechanisms. Additional testing is required to reach definitive conclusions regarding this effect.

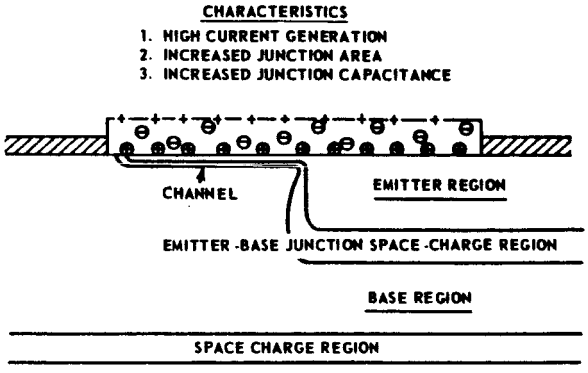
It is emphasized that the tests, test results, and conclusions discussed for Phase I were obtained with Fairchild 2N1613 transistors. These results cannot be extended to other oxide passivated planar devices because the magnitude and relative importance of different damage mechanisms are expected to vary. Some of these variations will be better understood after completion of Phase II.

3.3 MODEL

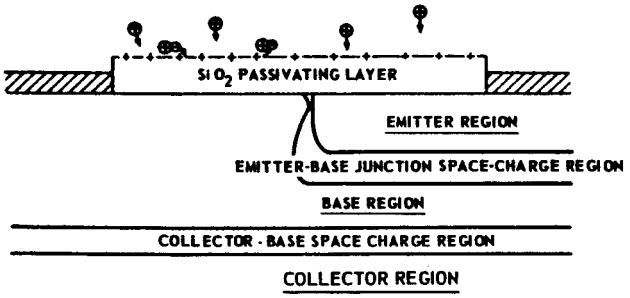
A model was proposed to explain the strong influence of collector-base reverse bias at early doses on the current gain h_{FE}, which is a base-emitter junction property. The model shown in Figure 12 is repeated from the Second Quarterly Report for reference. Since



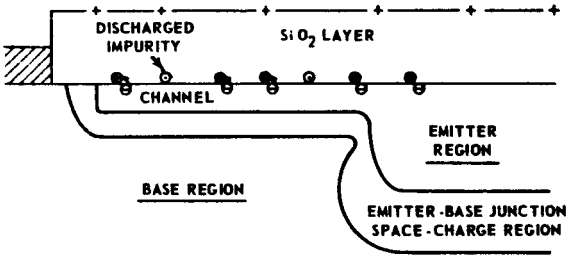
(a) Attraction of Positive Gas Ions To Base and Emitter Regions by Reverse Collector – Base Bias



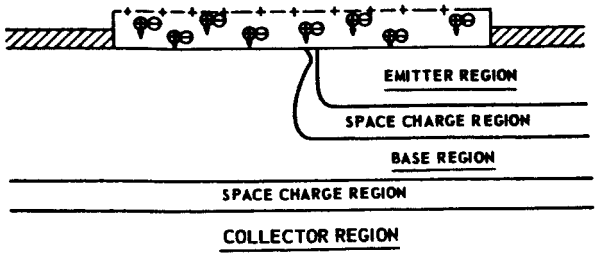
(d) Channel Induced by Accumulation of Positive Space Charge at the SiO_2 - Si Interface



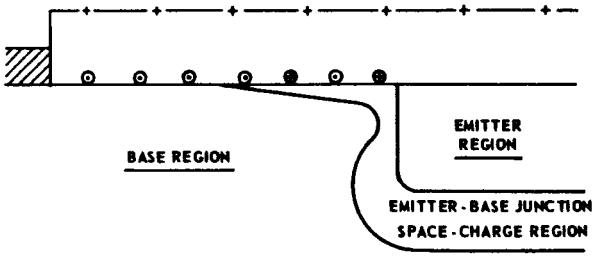
(b) Creation of SiO_2 Surface Space Charge by Interaction With Gas Ions



(e) Discharge of Positive Charge at SiO_2 - Si Interface by Electron Injection across Interface



(c) Migration of Ionized Species in the SiO_2 Layer Due to Surface Charge Induced Electric Field



(f) Recession of Channel Due to Discharge of Positive Interface Space Charge

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Figure 12 - Model for Ionizing Radiation Surface Effects

collection of positive charge via gas ions on the SiO_2 surface over a p region tends to deplete the p material at the surface, the question arises as to whether this surface charge is strong enough to cause inversion or a channel. Assuming that collection of SiO_2 surface charge continues until no electric field exists in the gas ambient above the oxide, the potential across the SiO_2 layer will approach that applied across the collector-base junction.

The SiO_2 layer over the base region on a Fairchild 2N1613 is from 4000 Å to 6000 Å thick, and the base surface concentration is from 2×10^{18} cm^{-3} to 5×10^{18} cm^{-3}.[2] Assuming no migration of charge within the oxide layer, the applied voltage necessary to invert the base surface is from 22 volts to 54 volts for the above conditions.[1] The 6 volt and 12 volt irradiations discussed for Test 5 did produce channels even though the potential across the oxide was less than 22 volts. This suggests that migration within the oxide did occur and that the channels were the result of a high electric field near the SiO_2-Si interface, consistent with the model of Figure 12. However, the direct inversion by surface charge may help explain the unexpected behavior of the 50 volt irradiation of Test 5, since this potential may be high enough to produce a channel without charge migration. This would modify the model by depicting a channel in Figure 12(c), rather than after charge migration as implied by delaying the channel formation until Figure 12(d).

SECTION 4

PHASE II TEST PLANS

The transistors that are to be tested in Phase II are specified in Contract NAS8-20135, EXHIBIT "A" Section I., SCOPE OF WORK. Phase II, which is described in Section I. B. of EXHIBIT "A" is divided into two categories: category (A) specifies particular structural design features of test devices, and (B) specifies particular devices. Table 1 lists the devices to be tested during Phase II, indicating the item of the contract which specifies the device. All deviations from contract specifications have been discussed with the Contract Technical Monitor, and explanations are given in footnotes to the table.

Based on the damage buildup characteristics observed in Phase I, the general test procedure adopted for Phase II is to bias the test devices with either (1) reverse-biased collector-base junctions which produce worst-case damage for bipolar transistors or (2) a specific operating condition that would be typical for the device. The devices so biased will be subjected to X-ray irradiation at a dose rate of approximately 1.67 r/hr, and damage buildup will be monitored by measuring I_{CBO} and/or collector-base junction capacitance in one or more pilot devices. This reduced dose rate is used to enable detection of channel buildup during the early irradiation period. If channels are induced in the test transistors, the bias-radiation stress will be stopped at the time that the induced channel reaches a maximum, and h_{FE}, I_{CBO} and reverse junction V-I data will be recorded. The bias-radiation stresses will be reapplied at a maximum dose rate of approximately 5×10^5 r/hr until the rate of damage buildup is very small (for about 10 to 16 hours). If no apparent channel can be induced in the test transistors, early data will be recorded after about 1/2 hour. If damage buildup is observed to be slow at $\dot{\phi} = 1.67 \times 10^5$ r/hr, the dose rate will be increased as soon as possible to $\dot{\phi} = 5 \times 10^5$ r/hr. This test procedure was determined from Phase I results based on the behavior of 2N1613 transistors. It is anticipated that not all devices will behave similarly to 2N1613s and that changes in the test procedure will be required.

A total of 13 devices of each type specified in Section I. B. (B) of EXHIBIT "A" will be tested (12 irradiated samples and one control sample);

Table 1 - Phase II Devices

Contract Specified Item EXHIBIT "A" I	Description	Device	Type
B.(A) 1.	Glass over oxide passivation	(3)	
B.(A) 2.	Special low current transistor	2N3058	Crystalonics, Nanowatt, Si, p-n-p
B.(A) 3.	Fairchild Planar II process	(3)	
B.(A) 4.	Texas Instruments field plate	2N1132 & 2N722	Included in B.(B) 3. and B.(B) 6.
B.(A) 5.	Motorola annular process	2N2222 or 2N2905	Included in B.(B) 2. and B.(B) 4.
B.(A) 6.	Motorola glass over metal over glass over oxide	(3)	
B.(B) 1.	2N2222 without annular ring	2N2222	Fairchild n-p-n
B.(B) 2.	2N2222 with annular ring	2N2222	Motorola n-p-n
B.(B) 3.	2N1132A without annular ring	2N1132 (1)	TI, p-n-p
B.(B) 4.	2N2905 with annular ring	2N2905	Motorola p-n-p
B.(B) 5.	2N1613	2N1613	Fairchild, n-p-n
B.(B) 6.	2N722	2N722 (4)	Motorola and TI, p-n-p also B.(A) 4.
B.(B) 7.	2N3387 junction type field effect	2N3387	Siliconex, ceramic flat package
B.(B) 8.	2N3609, MOS FET	2N3609	General Microelectronics
B.(B) 9.	2N2772	2N2771 (2)	Westinghouse n-p-n, Si, 200 W
B.(B) 10.	STC 1739	STC 1739	STC, n-p-n, Si, 200 W

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(1) 2N1132s are no longer manufactured without the annular ring; 2N1132As were unobtainable

(2) Equivalent device supplied by NASA

(3) Not yet selected

(4) Six test devices plus one control sample from each manufacturer.

no set number of devices is specified for those devices in I. B. (A). The contractor will test as many I. B. (A) devices as is feasible in keeping with obtaining significant data (from 6 to 12 irradiated samples).

The power devices, 2N2771 and STC1739, will be tested with biases, half of which correspond to their normal mode of operation and the other half with a reverse collector-base to produce worst-case damage. For these device types, the normal mode will be a switching mode achieved by a 400 c/s square wave base drive where I_C = 4.5 A, I_B = 400 mA during saturation and V_{CE} = 56 volts during cutoff.

Both the junction FET (2N3387) and the MOS FET (2N3609) will require special test considerations to evaluate these components for the worst-case operating point.

SECTION 5

FURTHER ACTIONS REQUIRED

The goals of Phase I have been accomplished, with the exception of the vacuum test. Phase II tests will be interrupted and this test conducted as soon as evacuated devices are fabricated. During Phase I investigations, several areas were encountered which require further study for a complete understanding of surface effects. They include:

(1) Rate effects

(2) Effects of different collector-base reverse bias magnitude during irradiation

(3) "Droop" damage component

(4) Temperature coefficient variations

(5) Damage stability

(6) Effect of radiation screening on device reliability.

It is anticipated that additional unresolved areas will be encountered during Phase II. Some of these problem areas will be investigated further after completion of Phase II, if time and funding permit.

SECTION 6

REFERENCES

1. D. J. Fitzgerald and A. S. Grove, "Mechanisms of Channel Current Formation in Silicon P-N Junctions," presented at Fourth Physics-of Failure Symposium, Chicago, November 1965.

2. David Meyers, Fairchild Semiconductor Division, private communication, April 1966.